REMARKS

Favorable reconsideration of this application in view of the remarks to follow is respectfully requested. Since the present Response raises no new issues, and in any event, places the application in better condition for consideration on appeal, entry thereof is respectfully requested under the provisions of 37 C.F.R. §1.116.

In this amendment, Applicants have added new independent Claim 40. Support for new Claim 40 is found throughout Applicants' specification. More specifically, support for each element of new Claim 40 is as follows:

> A method of fabricating a silicon-on-insulator substrate comprising:
> first ion implanting p-type or n-type dopants into a Si-containing substrate to a depth ranging from about 250 nm to about 1500 nm from a top surface of the Si-containing substrate; (*See paragraphs 35, 36, and 39 of Applicants' specification*)
>
> second ion implanting at least one ion selected from the group consisting of Si, Ge, Ne, Bi, Sn and Xe, wherein the at least one ion may be implanted to below, above or within the depth at which the p-type or n-type dopants are present in the Si-containing substrate; (*See paragraphs 40-41 of Applicants' specification*)
>
> annealing the n-type or p-type dopants to provide an activated n-type or p-type dopant region in the Si-containing substrate; (*See paragraphs 42-46 of Applicants' specification*)
>
> performing an electrolytic anodization process comprising immersing the Si-containing substrate into an Hf-containing solution and applying a current density ranging from about 0.05 milliAmps/cm^2 to about 50 milliAmps/cm^2 to the Si-containing substrate to produce a porous Si region having a porosity of about 0.01% or greater at a depth greater than 50 nm from the upper surface of the Si-containing substrate, wherein the electrolytic anodization process converts the activated n-type or p-type dopant region into the porous Si region; and (*See paragraphs 47-53 of Applicants' specification)*
>
> thermal oxidizing at a temperature ranging from about 650°C to about 1350°C to convert the porous Si region to a buried oxide region, wherein a portion of the Si-containing substrate overlying the buried oxide region provides a Si-containing overlayer. (*See paragraphs 58-62 of Applicants' specification)*

In light of new Claim 40, Claims 1-3, 7, 12-15, 25-26, 31-33 and 35-38 have been cancelled. Claims 8, 16, 18, 21-24, 27, 29, 34 and 39 have been amended to be consistent with the current amendment.

Applicants submit that the applied prior art fails to teach or suggest a method that includes the steps of first ion implanting p-type or n-type dopants into a Si-containing substrate to a depth ranging from about 250 nm to about 1500 nm from a top surface of the Si-containing substrate, second ion implanting at least one ion selected from the group consisting of Si, Ge, Ne, Bi, Sn and Xe, performing an electrolytic anodization process comprising immersing the Si-containing substrate into an Hf-containing solution to produce a porous region at a depth greater than 50 nm from the upper surface of the Si-containing substrate, and thermal oxidizing to convert a porous Si region to a buried oxide region, wherein a portion of the Si-containing substrate overlying the buried oxide region provides a Si-containing overlayer.

The applied prior art either provides a buried oxide layer by ion implantation of oxygen, wherein oxygen is not one of the elements included within the scope of new Claim 40; or the applied prior art utilizes electrolytic anodization to form a porous region on the surface of a substrate followed by a growth process to form the silicon layer atop the porous region in providing an SOI structure, which fails to meet the limitations of converting a porous Si region into a buried oxide region, wherein a portion of the Si-containing substrate overlying the buried oxide region provides a Si-containing overlayer, as recited in new Claim 40. Turning to the present grounds of rejection.

Claims 1-14, 16-24, 26-36 and 39 stand rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the written description requirement.

In light of the above amendments to the claims, Applicants respectfully request that the present 35 U.S.C. §112, first paragraph, rejections has been obviated, and respectfully request withdrawal thereof.

Claims 1-14, 16-24, 26-36 and 39 stand rejected under 35 U.S.C. §112, second paragraph, as allegedly indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention.

In light of the above amendments to the claims, Applicants respectfully request that the present 35 U.S.C. §112, second paragraph, rejections has been obviated, and respectfully request withdrawal thereof.

Claims 1-14, 16-24, 26, 35, 29-30 and 39 stand rejected, under 35 U.S.C. §103(a), as allegedly being unpatentable over JP 09-064323 to Ikeda ("Ikeda") in view of JP 62-245620 to Hiromitsu et al. ("Hiromitsu et al."). Applicants respectfully traverse for the following reasons.

Applicants submit that the applied prior art fails to render Applicants' invention obvious, since the applied prior art fails to teach or suggest each and every limitation of Applicants' claimed method, as recited in new Claim 40.

More specifically, Ikeda fails to teach or suggest a method of fabricating a silicon-on-insulator substrate comprising first ion implanting p-type or n-type dopants into a Si-containing substrate to a depth ranging from about 250 nm to about 1500 nm from a top surface of the Si-

containing substrate; second ion implanting at least one ion selected from the group consisting of Si, Ge, Ne, Bi, Sn and Xe, wherein the at least one ion may be implanted to below, above or within the depth at which the p-type or n-type dopants are present in the Si-containing substrate; annealing the n-type or p-type dopants to provide an activated n-type or p-type dopant region in the Si-containing substrate; performing an electrolytic anodization process comprising immersing the Si-containing substrate into an Hf-containing solution and applying a current density ranging from about 0.05 milliAmps/cm^2 to about 50 milliAmps/cm^2 to the Si-containing substrate to produce a porous Si region having a porosity of about 0.01% or greater at a depth greater than 50 nm from the upper surface of the Si-containing substrate, wherein the electrolytic anodization process converts the activated n-type or p-type dopant region into the porous Si region; and thermal oxidizing at a temperature ranging from about 650°C to about 1350°C to convert the porous Si region to a buried oxide region, wherein a portion of the Si-containing substrate overlying the buried oxide region provides a Si-containing overlayer, as recited in new Claim 40.

Applicants submit that Ikea requires the implantation of oxygen ions to provide a buried oxide layer and is far removed from Applicants' invention, which does not require or claim the implantation of oxygen ions. Referring to the abstract and Figure 1 of the Ikeda disclosure, Ikeda discloses a method that includes forming a porous silicon layer 22 by anodic formation and then growing epitaxial silicon on the porous silicon layer 22, wherein the epitaxial silicon provides the SOI layer, i.e. single crystal silicon layer 23. Therefore, since Ikeda requires a separate deposition of epitaxial Si to provide the SOI layer, Ikeda fails to teach or suggest a method that includes a process sequence of first ion implanting p-type or n-type dopants into a Si-containing substrate; second ion implanting at least one ion selected from the group consisting of Si, Ge, Ne, Bi, Sn and Xe, wherein the at least one ion may be implanted to below, above or within the depth

at which the p-type or n-type dopants are present in the Si-containing substrate; performing an electrolytic anodization process to produce a porous Si region having a porosity of about 0.01% or greater at a depth greater than 50 nm from the upper surface of the Si-containing substrate; and performing a thermal oxidation at to convert the porous Si region to a buried oxide region, wherein a portion of the Si-containing substrate overlying the buried oxide region provides a Si-containing overlayer, as recited in new Claim 40.

More specifically, because Ikeda discloses forming a porous region on the surface of a Si-containing substrate using anodization following by growing a Si containing layer atop the porous region, Ikeda fails to teach or suggest a method that forms a buried oxide region at a depth greater than 50 nm into a Si-containing substrate, wherein the portion of the Si-containing substrate atop the buried oxide region provides the Si containing overlayer, as required by new Claim 40. Applicants' further submit that Ikea fails to disclose one of the ions recited in new Claim 40 for the second ion implantation step.

Therefore, Ikeda fails to teach or suggest at least two required limitations of Applicants' claimed method, as recited in new Claim 40.

Hiromitsu fails to fulfill the deficiencies of Ikeda, because Hiromitsu also fails to teach or suggest each and every limitation of Applicants' method, as recited in new Claim 40. Hiromitsu discloses a method that forms a Si seed layer atop an insulating substrate. More specifically, Hiromitsu forms a Si-containing seed in an insulating layer, following by the deposition of an amorphous Si layer atop the insulating layer, wherein the Si-seed embedded in the insulating layer is utilized to convert the amorphous Si layer that is present atop the insulating layer into single crystal Si. Therefore, Hiromitsu is far removed from Applicants' method, because

Applicants' method forms a buried oxide layer in a silicon-containing substrate, as required by new Claim 40.

Specifically, Hiromitsu fails to teach or suggest a method of fabricating a silicon-on-insulator substrate comprising first ion implanting p-type or n-type dopants into a Si-containing substrate to a depth ranging from about 250 nm to about 1500 nm from a top surface of the Si-containing substrate; second ion implanting at least one ion selected from the group consisting of Si, Ge, Ne, Bi, Sn and Xe, wherein the at least one ion may be implanted to below, above or within the depth at which the p-type or n-type dopants are present in the Si-containing substrate; annealing the n-type or p-type dopants to provide an activated n-type or p-type dopant region in the Si-containing substrate; performing an electrolytic anodization process comprising immersing the Si-containing substrate into an Hf-containing solution and applying a current density ranging from about 0.05 milliAmps/cm^2 to about 50 milliAmps/cm^2 to the Si-containing substrate to produce a porous Si region having a porosity of about 0.01% or greater at a depth greater than 50 nm from the upper surface of the Si-containing substrate, wherein the electrolytic anodization process converts the activated n-type or p-type dopant region into the porous Si region; and thermal oxidizing at a temperature ranging from about 650°C to about 1350°C to convert the porous Si region to a buried oxide region, wherein a portion of the Si-containing substrate overlying the buried oxide region provides a Si-containing overlayer, as recited in new Claim 40.

In view of the above, Hiromitsu fails to teach or suggest at least two required limitations of Applicants' claimed method, as recited in new Claim 40.

Applicants submit that the §103 rejection of Claims 1-14, 16-24, 26, 35, 29-30 and 39 citing the combination of Ikeda and Hiromitsu has been obviated and request withdrawal thereof.

Claims 1-14, 16-24, 26, 29-30, 35-36 and 38 stand rejected, under 35 U.S.C. §103(a), as allegedly unpatentable over US2002/0086463 to Houston et al. ("Houston et al.") in view of JP 62-245620 to Hiromitsu ("Hiromitsu"). Applicants respectfully traverse for the following reasons.

Applicants submit that the applied prior art fails to render Applicants' invention obvious, since the applied prior art fails to teach or suggest each and every limitation of Applicants' claimed method, as recited in new Claim 40.

More specifically, the applied prior art fails to teach or suggest a method that includes a process sequence of first ion implanting p-type or n-type dopants into a Si-containing substrate; second ion implanting at least one ion selected from the group consisting of Si, Ge, Ne, Bi, Sn and Xe, wherein the at least one ion may be implanted to below, above or within the depth at which the p-type or n-type dopants are present in the Si-containing substrate; performing an electrolytic anodization process to produce a porous Si region having a porosity of about 0.01% or greater at a depth greater than 50 nm from the upper surface of the Si-containing substrate; and performing a thermal oxidation at to convert the porous Si region to a buried oxide region, wherein a portion of the Si-containing substrate overlying the buried oxide region provides a Si-containing overlayer, as recited in new Claim 40.

Referring to Paragraphs 0016, 0017 and Figure 1 of Houston et al., the applied reference discloses a method of forming a silicon on insulator substrate that includes the steps of providing a porous silicon region in the substrate by boron doping; epitaxial growth of a Si layer atop an the porous silicon surface; and implanting oxygen into the porous layer using a plasma oxygen implant or other oxygen implantation methods, wherein the implanted oxygen provides the

buried oxide layer. Applicants submit that Houston et al., which is reliant on the implantation of oxygen to produce a buried oxide layer, is far removed from Applicants' invention.

Therefore, since Houston et al. deposits an epitaxial Si layer atop a porous silicon region and then implants oxygen to provide a buried oxide layer, Houston et al. does not teach or suggest fails to teach or suggest a method that includes a process sequence of first ion implanting p-type or n-type dopants into a Si-containing substrate; second ion implanting at least one ion selected from the group consisting of Si, Ge, Ne, Bi, Sn and Xe, wherein the at least one ion may be implanted to below, above or within the depth at which the p-type or n-type dopants are present in the Si-containing substrate; performing an electrolytic anodization process to produce a porous Si region having a porosity of about 0.01% or greater at a depth greater than 50 nm from the upper surface of the Si-containing substrate; and performing a thermal oxidation at to convert the porous Si region to a buried oxide region, wherein a portion of the Si-containing substrate overlying the buried oxide region provides a Si-containing overlayer, as recited in new Claim 40.

Houston et al. fails to teach or suggest at least two required limitations of Applicants' claimed method, as recited in new Claim 40.

Applicants note that Hiromitsu fails to alleviate the deficiencies in Houston et al., because Hiromitsu also fails to teach or suggest each and every limitation of Applicants' method, as recited in new Claim 40. The deficiencies of Hiromitsu discussed above are equally applicable to the present rejection.

Applicants submit that the §103 rejection of Claims 1-14, 16-24, 26, 29-30, 35-36 and 38 citing Houston et al. and Hiromitsu has been obviated and request withdrawal thereof, since the applied prior art alone or in combination fails to teach or suggest Applicants' claimed method, as recited in new Claim 40.

Claims 1-3, 12, 14, 16-24, 26 and 31-36 stand rejected under 35 U.S.C. §102(e) as allegedly anticipated by or, in the alternative, under 35 U.S.C. §103(a), as allegedly obvious over U.S. Patent No. 6,800, 518 to Bendernagel et al. ("Bendernagel et al.").

Applicants submit that the applied prior art fails to anticipate or render obvious Applicants' claimed invention, since the applied prior art fails to teach or suggest each and every limitation of Applicants' claimed method, as recited in new Claim 40.

Specifically, the applied prior art fails to teach or suggest a method that includes a process sequence of first ion implanting p-type or n-type dopants into a Si-containing substrate; second ion implanting at least one ion selected from the group consisting of Si, Ge, Ne, Bi, Sn and Xe, wherein the at least one ion may be implanted to below, above or within the depth at which the p-type or n-type dopants are present in the Si-containing substrate; performing an electrolytic anodization process to produce a porous Si region having a porosity of about 0.01% or greater at a depth greater than 50 nm from the upper surface of the Si-containing substrate; and performing a thermal oxidation at to convert the porous Si region to a buried oxide region, wherein a portion of the Si-containing substrate overlying the buried oxide region provides a Si-containing overlayer, as recited in new Claim 40.

Referring to Column 3, lines 40-60, and Figure 1 of Bendernagel et al., Bendernagel et al. discloses a method that includes forming a layer of porous Si on the surface of a semiconductor wafer 10, forming an epi-Si layer 30 on the layer of porous Si; selectively implanting ions into predetermined areas of the wafer 10 to form implant regions at or near said interface; and annealing the wafer at an elevated temperature which causes transformation of the implant

regions, by reaction with the surrounding layer of porous Si, into buried insulating regions 26, and transformation of unimplanted porous Si, by pore coalescence, into buried void planes 27.

Referring to Column 3, lines 15-30, and Figure 1, Bendernagel et al. discloses a structure that includes a semiconductor substrate 10; one or more layers of patterned buried insulating regions 26 and void planes 27 located next to each other and atop the semiconductor substrate 10; and a Si over-layer 30 located atop the one or more layers of patterned buried insulating regions 26 and void planes 27.

Therefore, since Bendernagel et al. produces a SOI layer by epitaxial formation, Bendernagel et al. fails to teach or suggest a method that includes a process sequence of first ion implanting p-type or n-type dopants into a Si-containing substrate; second ion implanting at least one ion selected from the group consisting of Si, Ge, Ne, Bi, Sn and Xe, wherein the at least one ion may be implanted to below, above or within the depth at which the p-type or n-type dopants are present in the Si-containing substrate; performing an electrolytic anodization process to produce a porous Si region having a porosity of about 0.01% or greater at a depth greater than 50 nm from the upper surface of the Si-containing substrate; and performing a thermal oxidation at to convert the porous Si region to a buried oxide region, wherein a portion of the Si-containing substrate overlying the buried oxide region provides a Si-containing overlayer, as recited in new Claim 40.

Applicants submit that the §102 and §103 rejections of Claims 1-3, 12, 14, 16-24, 26 and 31-36 citing Bendernagel et al. have been obviated and request withdrawal thereof.

Claims 4-11, 13 and 39 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Bendernagel et al., optionally in view of Hiromitsu. Applicants traverse the aforementioned rejection and submit the following.

"To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art". *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970). If an independent claim is non-obvious under 35 U.S.C. §103(a), then any claim depending therefrom is non-obvious. *In re Fine,* 837F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Claims 4-11, 13 and 39 are now dependent on new Claim 40. The failure of Bendernagel et al. and Hiromitsu to render new Claim 40 unpatentable is discussed above, and is incorporated into the discussion of the present rejection by reference. Therefore, because the applied prior art fails to render the base claim unpatentable, i.e., new Claim 40, the applied prior art fails to render dependent Claims 4-11, 13 and 39 unpatentable.

Applicants submit that the present §103 rejections of Claims 4-11, 13 and 39 have been obviated and request withdrawal thereof.

Claims 1-14 16, 24, 26, 31-36 and 39 stand rejected on the ground of non-statutory obviousness-type double patenting as allegedly unpatentable over Claims 14-38 of U.S. Patent No. 6,800,518 B2 to Bendernagel et al. ("Bendernagel et al."), optionally in view of U.S. Patent No. 5,930, 643 to Sadana et al. ("Sadana et al.") and JP 62-245620 to Hiromitsu et al. ("Hiromitsu et al."). Applicants respectfully traverse for the following reasons.

Applicants are in the process of preparing a corrected and signed PTO/SB/25 (09-04) terminal disclaimer form to obviate the non-statutory obviousness type double patenting over

claims 1-14 of U.S. Patent No. 6,800,518 to Bendernagel et al. We will forward a signed copy of the above noted form upon receipt.

Sadana et al. fails to disclose performing an electrolytic anodization process, as recited in new Claim 40. Sadana et al. discloses a method that includes implanting oxygen ions into a surface of a semiconductor substrate to form a stable buried damaged region, and is far removed from Applicants' claimed method. There is no disclosure of anodization throughout the Sadana et al. reference. Therefore, Sadana et al. fails to teach or suggest each and every element of Applicants' claimed method, as recited in new Claim 40.

The failure of Hiromitsu to render new Claim 40 unpatentable is discussed above, and is incorporated into the discussion of the present rejection by reference.

Claims 1-14, 18-24, 26-28, 31-36 and 39 stand rejected under 35 U.S.C. §103(a) as allegedly obvious over U.S. Patent No. 5,387, 541 to Hodge et al. ("Hodge et al.") in view of Hiromitsu et al. Applicants traverse the aforementioned rejection and submit the following.

Applicants submit that the Hodge et al. fails to render Applicants' invention obvious, since Hodge et al. fails to teach or suggest each and every limitation of Applicants' claimed method, as recited in new Claim 40. Specifically, Hodge et al. fails to teach or suggest a method of fabricating a silicon-on-insulator substrate including a process sequence of first ion implanting p-type or n-type dopants into a Si-containing substrate; second ion implanting at least one ion selected from the group consisting of Si, Ge, Ne, Bi, Sn and Xe, wherein the at least one ion may be implanted to below, above or within the depth at which the p-type or n-type dopants are present in the Si-containing substrate; performing an electrolytic anodization process to produce a porous Si region having a porosity of about 0.01% or greater at a depth

greater than 50 nm from the upper surface of the Si-containing substrate; and performing a thermal oxidation at to convert the porous Si region to a buried oxide region, wherein a portion of the Si-containing substrate overlying the buried oxide region provides a Si-containing overlayer, as recited in new Claim 40.

Hodge et al. discloses a process that includes providing a porous silicon layer by anodization (see Figures 1-2, and column 2, line 35, to column 3, line 5, of Hodge et al. reference); ion implantation to produce an amorphous region in the porous Si (see Figures 1 and 2, and column 3, lines 5-35 of the Hodge et al. reference); and annealing to recrystallize the amorphous Si in providing the SOI layer of a silicon on insulator substrate (see Column 3, lines 35-65 of the Hodge et al. reference). The sequence disclosed in Hodge et al. fails to meet Applicants' claimed method, because Hodge et al. produce a porous Si region by anodization prior to ion implantation. Contrary to the method disclosed in Hodge et al., Applicants' method includes a first implant of n-type or p-type dopants, as well as a second implant of an ion selected from the group consisting of Si, Ge, Ne, Bi, Sn and Xe, prior to electrolytic anodization, as recited in new Claim 40.

Hodge et al. also fails to teach forming an SOI layer during oxidation. Instead, Hodge et al. relies on a recrystallization step to grow an SOI layer from an amorphous Si region, which does not meet the limitation of an oxidation step that provides both the SOI layer and buried oxide layer, as required by new Claim 40. Although, Hodge et al. discloses embodiments including oxidation steps following and prior to the formation of the SOI layer, in each of the embodiments disclosed Hodge et al. is relying on a separate anneal step in a non-oxidizing environment, i.e., an anneal including argon or nitrogen anneal (see column 3,

lines 60-65, of the Hodge et al.), to produce the SOI layer from a recrystallized growth of Si from an amorphous Si region.

Therefore, since Hodge et al. relies on a separate anneal to provide an SOI layer from recrystallized Si growth, Hodge et al. fails to teach or suggest a method that includes a process sequence of first ion implanting p-type or n-type dopants into a Si-containing substrate; second ion implanting at least one ion selected from the group consisting of Si, Ge, Ne, Bi, Sn and Xe, wherein the at least one ion may be implanted to below, above or within the depth at which the p-type or n-type dopants are present in the Si-containing substrate; performing an electrolytic anodization process to produce a porous Si region having a porosity of about 0.01% or greater at a depth greater than 50 nm from the upper surface of the Si-containing substrate; and performing a thermal oxidation at to convert the porous Si region to a buried oxide region, wherein a portion of the Si-containing substrate overlying the buried oxide region provides a Si-containing overlayer, as recited in new Claim 40.

The failure of Hiromitsu to render new Claim 40 unpatentable is discussed above, and is incorporated into the discussion of the present rejection by reference.

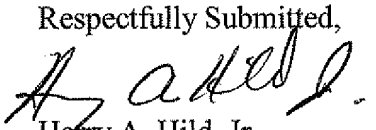
Applicants submit that the §103 rejection of Claims 1-14, 18-24, 26-28, 31-36 and 39 citing the combined disclosures of Hodge et al. and Hiromitsu have been obviated and request withdrawal thereof.

Applicants are in the process of preparing a corrected and signed PTO/SB/25 (09-04) terminal disclaimer form to obviate the non-statutory obviousness type double patenting over Claims 1, 14, 16-24, 26, 31-33, 35-36 and 38 of over claims 1-39 of U.S. Patent No. 6, 486, 037, to Norcott et al. We will forward a signed copy of the above noted form upon receipt.

Accordingly, the Examiner is respectfully requested to reconsider the application, withdraw the rejections and issue an immediate a favorable action thereon. If upon review of the application, the Examiner is unable issue an immediate Notice of Allowance, the Examiner is respectfully requested to telephone the undersigned with a view towards resolving any outstanding issues.

An early and favorable action is earnestly solicited.

Respectfully Submitted,



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